IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A storage device, comprising:

a memory;

a microcomputer for taking in data read from the memory according to a externally-supplied clock signal or a clock signal generated based on the externally-supplied clock signal;

a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a predetermined time period, which is determined according to a frequency of the clock signal, from a predetermined edge in a read control signal which is used for controlling reading of data from the memory; and

a read data control circuit for performing control such that the microcomputer takes in the data read from the memory based on the timing signal only when the clock signal has a predetermined frequency between an upper limit and a lower limit determined according to the shift of the timing.

2. (Original) The storage device of claim 1, wherein the read data control circuit controls based on the timing signal at least any one of the followings:

whether or not the data read from the memory is output to the microcomputer;

the timing for outputting the data read from the memory to the microcomputer; and

the timing for taking the data read from the memory into the microcomputer.

3. (Original) The storage device of claim 2, wherein the read data control circuit controls whether or not the data read from the memory is output to the microcomputer based on the relationship between the timing which is indicated by the timing signal and the timing at which an edge subsequent to the predetermined edge occurs in the read control signal.

4. (Original) The storage device of claim 3, wherein when the read data control circuit does not output the data read from the memory to the microcomputer, the read data control circuit outputs data different from the data read from the memory.

5. (Original) The storage device of claim 2, wherein the read data control circuit outputs the data read from the memory to the microcomputer for a predetermined time period that is determined according to the timing signal.

6. (Original) The storage device of claim 5, wherein the read data control circuit outputs data different from the data read from the memory during a time period other than the predetermined time period.

7. (Original) The storage device of claim 2, further comprising a mask circuit for outputting the data read from the memory to the microcomputer for a predetermined time period,

wherein the read data control circuit performs control such that the microcomputer takes in data output from the mask circuit at a predetermined timing that is determined according to the timing signal.

8. (Original) The storage device of claim 7, wherein the mask circuit outputs data different from the data read from the memory during a time period other than the predetermined time period.

9. (Original) The storage device of claim 1, further comprising a temperature detection circuit,

wherein the read data control circuit performs control such that the microcomputer takes in the data read from the memory only when the temperature detection circuit detects a predetermined temperature.

10. (Original) The storage device of claim 1, further comprising a light detection circuit,

wherein the read data control circuit performs control such that the microcomputer takes in the data read from the memory only when the light detection circuit detects light having a predetermined intensity.

11. (Currently Amended) A storage device, comprising:

a memory;

a microcomputer for taking in data read from the memory according to a externally-supplied clock signal or a clock signal generated based on the externally-supplied clock signal;

a mask circuit for outputting the data read from the memory to the microcomputer for a predetermined time period; and

a timing control circuit for performing control such that the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer correspond to each other and are variable.

12. (Original) The storage device of claim 11, wherein the timing control circuit sets the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer, based on at least any one of the followings:

data retained in a predetermined area of the memory;

an address output from the microcomputer; and

a predetermined signal output from the microcomputer.